Computer Systems and Networks

ECPE 170 – Jeff Shafer – University of the Pacific

Exam 2 Review

Exam 2

- Similar format as last time
  - Closed notes, closed book, no calculator, etc…
  - **I will provide Table 4.7 (MARIE ISA)**
- **Chapter 4 – On the exam!**
- **Chapter 5 – On the exam!**

Review Materials

- Things to study
  - Homework assignments
    - **Solutions are posted in Sakai**
  - Quiz 3 and 4
    - **Solutions are posted in Sakai**
  - Lecture notes
- Question format will be similar to quizzes
  - Mix of problems and short answer questions
  - *Problems typically come from textbook…*
  - *Short answer questions typically come from lectures…*

Chapter 4 – Computer Organization

Exam 2

- **Chapter 4 Topics**
  - Basic computer organization
  - MARIE architecture
    - Major components and operation
  - MARIE programs
    - **"Write a complete program that does XYZ"**
    - Subroutines, indirect instructions, etc..

Computer Organization

- **What is a bus?**
- **What does the *clock* do?**
- **Is increasing the clock rate the only way to improve application performance?**

$$\text{CPU Time} = \frac{\text{seconds}}{\text{program}} = \frac{\text{instructions}}{\text{program}} * \frac{\text{avg.cycles}}{\text{instruction}} * \frac{\text{seconds}}{\text{cycle}}$$

Reduce any of these, or all three!

Computer Organization

- **What does *addressability* mean in the context of a memory system?**
- **Which type of memory system would require more address lines to access the same number of bytes: a *word-addressable* memory, or a *byte-addressable* memory?**
- **What is the difference between *high-order* and *low-order* interleaving? (What is interleaving?)**

Memory Organization

- Exercise: Build a 1M x 16 word-addressable main memory using 128K x 4 RAM chips.
  1. **How many address bits are needed per RAM chip?**
  2. **How many RAM chips are there per word?**
  3. **How many RAM chips are necessary?**
  4. **How many address bits are needed for all memory?**
  5. **How many address bits would be needed if it were byte addressable?**
  6. **How many banks will there be?**
  7. **What bank would contain address 47129_{16} with (a) high-order interleaving or (b) low-order interleaving?**

Solution to Exercise

1. Each RAM chip has 128K locations: $2^7 * 2^{10}$ = **17 bits**
2. Each RAM chip location stores 4 bits, but we need 16:
   1. **4 chips needed per word**
3. Each RAM chip has 128K locations, but we need 1M locations:
   1. 1M/128K = 8 (times 4 chips per word) = **32 RAM chips** (8 rows, 4 columns)
4. Memory is 1M: 2^20 = **20 bits for all of memory**
5. Byte addressable adds 1 more bit here (to select either the lower 8 or upper 8 of the 16 bit long word): **21 bits**
6. **8 banks** of memory, where each bank has 4 chips
7. Address is 20 bits long, bank is upper 3 bits (2^3=8):
   47129(16) = 0100 0111 0001 0010 1001 (2)
   With high-order interleaving, bank is **#2**
   With low-order interleaving, bank is **#1**

MARIE Components

- AC?
- PC?
- IR?
- ALU?
- MAR?
- MBR?

Chapter 5 - ISA

Exam 2

- **Chapter 5 Topics**
  - Endianness
  - Infix and postfix notation
  - Memory addressing modes
  - Pipelines (concept, speedup, hazards)
  - Instruction sets
    - 0-address machines (i.e. stack machines)
    - 1-address machines (i.e. accumulator machines)
    - 2-address and 3-address machines (general purpose register machines)
  - 7 different instruction types (data movement, arithmetic, etc…)

Pipeline Hazards

- In computer architecture, hazards are opportunities for data corruption and incorrect calculations if a naïve pipeline design does not detect specific error conditions and accommodate them, potentially by introducing delays ("stalls") in the pipeline.
- **What is a**
  - **Data hazard?**
  - **Structural hazard?**
  - **Control hazard?**

50 word Problem

- Data hazards represent obstacles preventing perfect parallel execution of instructions, such as when one instruction depends on a result produced by a previous instruction that has not yet finished (*a data hazard*), when multiple instructions rely on the same hardware element like a shared memory (*a structural hazard*), or when the next pipeline instruction cannot be immediately determined due to a yet-unresolved branch (*a control hazard*).
  - 66 words