Computer Systems and Networks

ECPE 170 – Jeff Shafer – University of the Pacific

Instruction Set Architecture

Schedule

- **Today**
  - Review HW #12, Quiz #3 (MARIE programming)
  - **Quiz 4**
- **Next Week**
  - **Spring break!**

Homework 5.18

- **Addressing modes – what is loaded in the accumulator?**
  - Instruction: LOAD 500
  - Contents of memory:
  - Contents of R1: 200
- Value in ACC for:
  - **Immediate mode?**
  - **Direct mode?**
  - **Indirect mode?**
  - **Indexed mode?**

Address	Data
100	600
400	300
500	100
600	500
700	800

Homework 5.19

- **Speedup of a pipelined system? (both with infinity instructions and with finite instructions)**
- Scenario
  - Non-pipelined system: 200ns per instr (t_n)
  - Pipelined system: 40ns per stage (t_p)
  - Pipeline depth: 5
- **Theoretical speedup**
  - **For ∞ instructions?**
  - **For 200 instructions?**

$$S = \frac{nt_n}{(k+n-1)t_p} = \frac{200 \times 200ns}{(5+200-1)\times 40ns} = 4.90$$

Recap – Pipeline Pitfalls

- **Why might we not achieve this full speedup in a pipelined system?**
  - Unbalanced pipeline: We *assumed* that a 200ns-per-instruction unpipelined system could be converted to a 5-stage 40ns-per-stage system
    - If the pipeline stages aren't perfectly balanced, we have to clock at the slowest stage
    - We might only be able to achieve 50 or 60ns per stage…
  - **Hazards**
    - Data hazards / structural hazards / control hazards

Homework 5.22

- **Write A = (B+C) x (D+E)** on:
  - 3-address machine (i.e. “mainframe”)
  - 2-address machine (i.e. modern RISC/CISC)
  - 1-address machine (i.e. **accumulator** machine)
  - 0-address machine (i.e. **stack** machine)
- Restriction: B, C, D, E should not be changed while performing this computation

Quizzes

- Review Quiz #3
- Take Quiz #4